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A novel high-precision curvature-compensated CMOS bandgap reference without using an op-amp

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ABSTRACT*:* A novel high-precision curvature-compensated bandgap reference (BGR) without using op-amp is presented in this paper. It is based on second-order curvature correction principle, which is a weighted sum of two voltage curves which have opposite curvature characteristic. One voltage curve is achieved by first-order curvature-compensated bandgap reference (FCBGR) without using op-amp and the other found by using W function is achieved by utilizing a positive temperature coefficient (TC) exponential current and a linear negative TC current to flow a linear resistor. The exponential current is gained by using anegative TC voltage to control a MOSFET in sub-threshold region. In the temperature ranging from -40℃ to 125℃, experimental results implemented with SMIC 0.18μm CMOS process demonstrate that the presented BGR can achieve a TC as low as 2.2 ppm/℃ and power-supply rejection ratio(PSRR)is -69 dB without any filtering capacitor at 2.0 V. While the range of the supply voltage is from 1.7 to 3.0 V, the output voltage line regulation is about1 mV/ V and the maximum TC is 3.4 ppm/℃.

Keywords: bandgap reference circuit, high precision, sub-threshold region, second-order curvature-compensation

I. INTRODUCTION

Recently, high-precision BGR is an essential building block for many applications ranging from purely analog, mixed-mode to purely digital circuits, such as data converters, DRAM, power converters, oscillators, flash memory controlling circuits, etc. Traditional BGR [1] is a weighted sum of positive TC thermal voltage VT and negative TC voltage VBE which is the base-emitter voltage of forward-biased BJT. Due to the nonlinearity of voltage VBE, the TC of traditional BGR is always confined between 20 and 100 ppm/°C [2]. In order to reduce the TC of traditional BGR, lots of works have been done. Based on BiCMOS process, an exponential compensation technique [3] and a piecewise technique [2] are introduced. They reduce the TC of corresponding circuit, but the higher requirements to the manufacturing process are necessary. Hereafter, The compensation method without resistances [4, 5] and the high-order curvature-compensated method [6] are adopted in the circuit. They can be compatible with standard CMOS technology and can improve the circuit accuracy, but the use of the op-amp increases complexity of the circuits.

In this paper, a high-precision BGR without op-amp is presented, which can be fabricated in standard CMOS process. Firstly, one compensated curve is obtained by a first-order curvature-compensated BGR (FCBGR) without using op-amp. Then, the MOSFET working in sub-threshold region is controlled by using a negative TC voltage to produce a positive TC exponential current. Later, a negative TC linear current is added with this exponential current to generate the second-order compensation current (SCC) which is proved to have curvature-up characteristic by Lambert W function. It is noted that the curvature characteristic of SCC and that of the FCBGR voltage are opposite. Therefore, the temperature drift of the presented BGR voltage is effectively reduced with using this compensation technique.

II. THE PRESENTED CURVATURE-COMPENSATED TECHNIQUE

The compensation procedure schematic diagram of the proposed BGR is shown in Fig. 1. In Fig. 1 (a), thermal voltage V_T and V_{BE} are used to generate the FCBGR voltage curve. Due to the nonlinearity of V_{BE}, the FCBGR voltage curve shows the curvature-down characteristic. In this paper, we give a temperature compensating voltage item as shown in Fig. 1 (b) to compensate the FCBGR voltage.

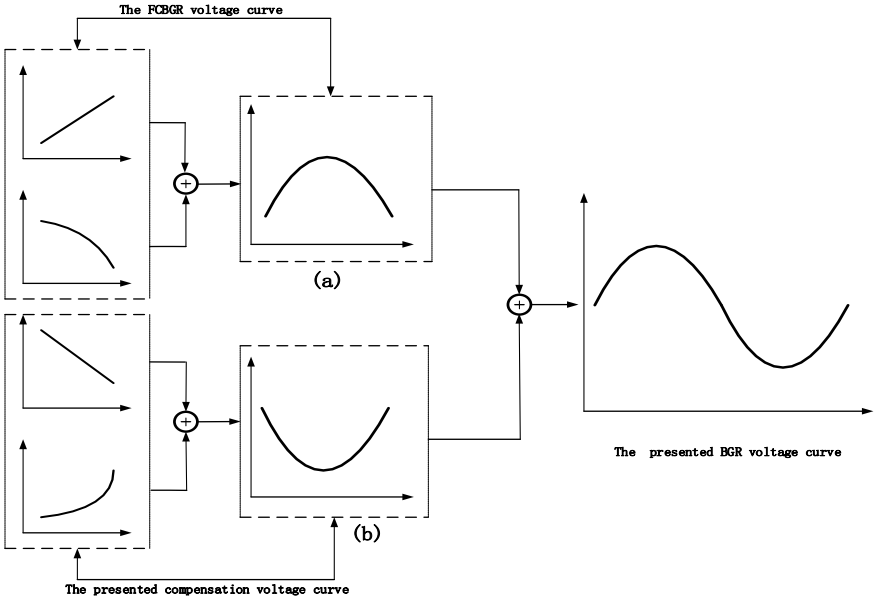


Fig. 1 The compensation procedure of the proposed BGR.

Based on the above scheme, the specific circuit implementation is shown in Fig. 2, where the presented circuit consists of a start-up circuit, a FCBGR generator, an exponential current generator and an I_{CTAT} generator.

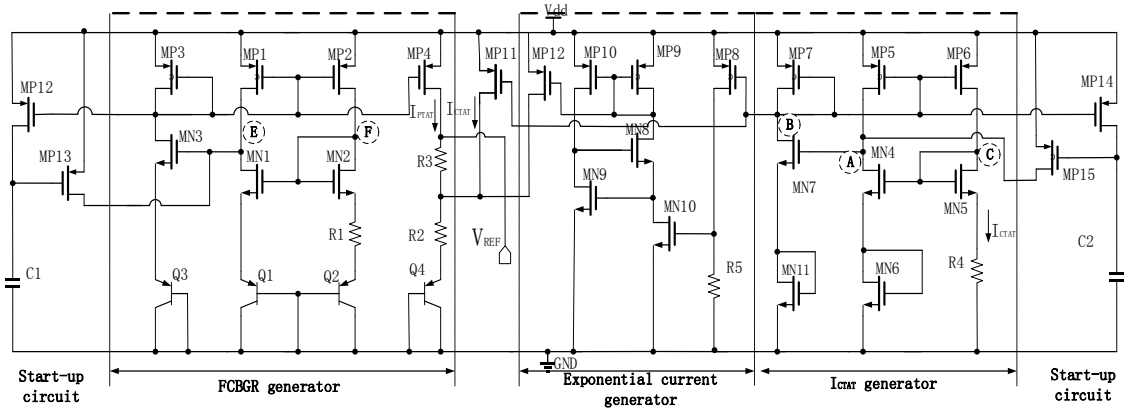


Fig.2 The proposed BGR circuit.

2.1 The principleof FCBGR generator

The FCBGR generator is givenon the left side ofFig. 2. In the past references [1, 4, 6], node E and F are generally stabilized by using op-amp. The scheme of this paper is to use a feedback loop [7] made by Q3, MN3, MP3, MP1 and MP2 to keepvoltage of node E andF equal, which can simplify the circuit design and improve PSRR. Devices MP1, MP2, MN1, MN2, Q1, Q2 and R1 are used to produce the PTAT current,where MP1 and MP2 have the same aspect ratio, and MN1 and MN2 have the same aspect ratio. Based onKirchhoff's law,we can obtain the following formulaas

$$V_{GS(MN1)} + V_{EB1} = V_{GS(MN2)} + V_{EB2} + I_{PTAT}R_1, \qquad (1)$$

where V_{EB1} and $V_{EB2}$are the emitter-base voltages of transistors Q1 and Q2. I_{PTAT} is proportional to the absolute temperature (PTAT) current. All of MOSFETs in FCBGR circuit work in the strong inversion region. Therefore, their gate-source voltage V_{GS} can be expressed in terms of their drain current $I_D$as follows

$$V_{GS} = V_{TH} + \sqrt{2I_D / \mu_n C_{ox}(W/L)}\,. \qquad (2)$$

Substituting (2) into (1), we get

$$I_{PTAT} = [(V_{EB1} - V_{EB2}) / R_1] = V_T \ln(E) / R_1, \qquad (3)$$

whereE is the emitter ratio ofQ2 and Q1. To simplify the analysis, we assume that for the same type of MOSFET, their threshold voltages are equal. Given $(W/L)_{MP4} = M_1(W/L)_{MP1} = M_1(W/L)_{MP2}$,the current ratio of MP4, MP1 and MP2 is $I_{MP4}=M_1I_{MP1}=M_1I_{MP2}$. Therefore, the FCBGR voltage can be given by

$$V_{REF1} = [M_1 V_T \ln(E) / R_1] \cdot (R_2 + R_3) + V_{EB4}, \quad (4)$$

where$V_{EB4}$is the emitter-base voltage of Q4. By properly selecting the valueof M1, R1, R2, R3 and E, the FCBGR can achieve mutual compensation of the FCBGR voltage. It should be noted that the Q3, MN3, MP3, MP2, MN2 and MN1 form a negative feedback loop, effectivelyimprovingthe stability of the circuit and PSRR.

2.2 The principle of SCC generator

As shown in the right ofFig. 2, the exponential current generator and I_{CTAT} generator compose the SCC generator. Voltage of R4is the threshold voltage $V_{TH(MN6)}$ [7]. $V_{TH(MN6)}= V_{TH0(MN6)}-\alpha V_T(T-T_0)$, where$\alpha V_T$ ($\alpha V_T>0$) is TC of the threshold voltage, $T_0$is the reference temperature and $V_{TH0}$is the threshold voltage at T_0. Thus, $I_{CTAT}=V_{TH(MN6)}/R_4$, which is complementary to absolute temperature. Given $(W/L)_{MP8}=M_2(W/L)_{MP6}$, the current ratio of MP8 and MP6 is $I_{D8}=M_2I_{D6}$. The voltage of R_5 can be expressed as

$$V_5 = \beta \cdot V_{TH(MN6)} = \beta[V_{TH0(MN6)} - \alpha_{VT}(T - T_0)] = V_{GS10}, \quad (5)$$

where $\beta=M_2R_5/R_4$, which is a coefficient independent of the temperature. To make MN10 work in the sub-threshold region, we have$V_{GS(MN10)}<V_{TH(MN10)}$, i.e.$\beta<1$. The drain current I_{D10} of MN10 operating in the sub-threshold region is given by [8]

$$I_{D10} = \mu_n C_{ox}(n-1)K_{10}V_T^2 \exp[(V_{GS} - V_{TH})/nV_T], \quad (6)$$

where n is the sub-threshold slope factor, μ_n is the carrier mobility($\mu_n=\mu_0 (T/T_0)^{-m}$), μ_0 is a temperature-independent constant,m is an empirical parameter associated with the process which is from 1.5 to 2[5], C_{ox} is the gate-oxide capacitance, and K_{10} is the aspect ratio of MN10.Substituting (5) into (6), the exponential compensation current I_{D10}can be rewrittenas

$$I_{D10} = B \cdot \exp(C / nT). \quad (7)$$

In(7), $B = \mu_0 T_0^2 C_{ox}(n-1)(W/L)_{MN10}(k^2/q^2)\exp[(1-\beta)\alpha_{VT} \cdot q/nk] > 0$, and $C = [(\beta-1) \cdot V_{TH0} + (\beta-1)\alpha_{VT} T_0 q/k] < 0$. Here, B and C are independent of temperature. It is easy to find that ID10 is a positive TC exponential current. Given $(W/L)_{MP11}=M_3(W/L)_{MP6}$ and $(W/L)_{MP12}=M_4(W/L)_{MP9}$, the current ratio of MP11 and MP6, MP12 and MP9are $I_{D11}=M_3I_{D6}$, $I_{D12}=M_4I_{D9}$, respectively. The SCC summed by I_{D11} and I_{D12}can be given by

$$I_{SCC} = M_4 B \cdot \exp(C / nT) + M_3 V_{TH(MN6)} / R_4. \quad (8)$$

In (8), we derive the first derivative of the current I_{SCC} and make it zero, and thus, we can get the following equation

$$M_4 B \cdot \exp(C / nT) \cdot (C / n) \cdot (-1/T^2) - A = 0, \quad (9)$$

where $A=\alpha V_T \cdot M_3/R_4$. By simplifying (9), when making the first derivative of I_{SCC} with respect toT_1zero, T_1 is obtained by using the Lambert W function [9] as

$$T_1 = (C/2n) \cdot \{1/W_0[\frac{C}{2n}\exp(-D)]\}. \quad (10)$$

Here, $D=\ln(-M_4 \cdot B \cdot C/nA)/2$, and W_0 is the notation of the principal-branch solution of theLambert W function. The second derivative of I_{SCC} can be expressed as

$$\frac{d^2 I_{SCC}}{dT^2} = \frac{M_4 B}{T^2}\exp(\frac{C}{nT})\frac{C}{nT}(\frac{C}{nT} + 2). \quad (11)$$

Over the entire temperature range, if C value is properly designed as C <-2nT, in (8), there is a zero first derivative in (10) and the second derivative in(11) is positive. Therefore, we can conclude that the SCC curve is the parabola-like going upwards. The presented BGR voltage VREF2 can be obtained as

$$V_{REF2} = [(R_2 + R_3) \cdot M_1 V_T \ln(E)/R_1 + R_2 M_3 V_{TH(MN6)}/R_4] + [V_{EB4} + R_2 M_4 B \cdot \exp(C/nT)]. \quad (20)$$

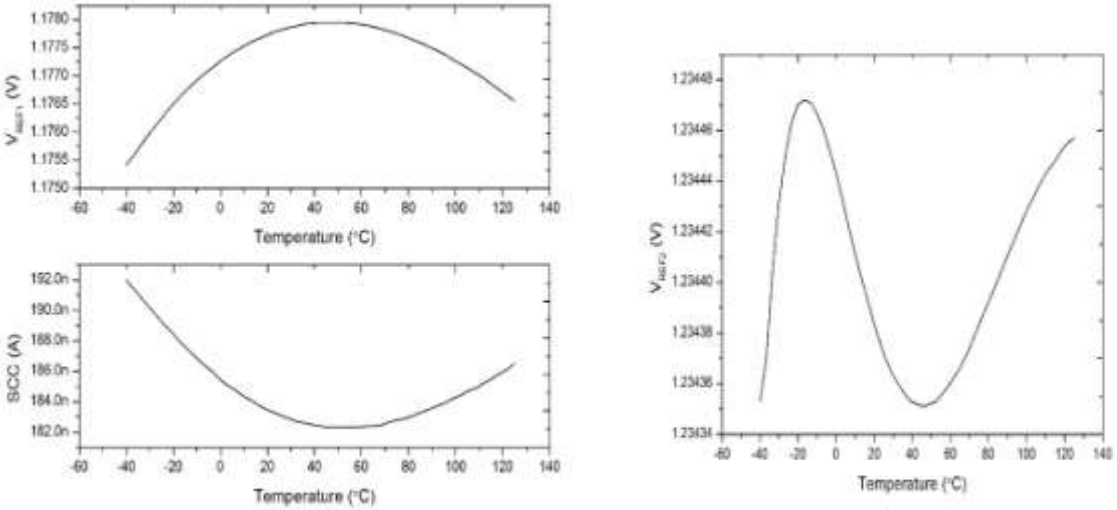
Therefore, we can get a high-precision BGR voltage based on the above compensation principle.

In order to make the MOSFET in the sub-threshold region work more stable over the entire temperature range and supply voltage variations, there are two considerations in the design of the circuit. For the first one, the negative feedback loop made by MN9, MP10, MP9, and MN8 is added to stabilize the drain-source voltage of MN10. As we know, the drain-source voltage affects the drain current. For the other consideration, we use the threshold voltage having a negative TC to generate a complementary to the absolute temperature current. Compared to other parameters having a negative temperature coefficient, the control voltage is generated by the threshold voltage, which is used to control the MOSFET in sub-threshold region and has a better process

matching. As indicated by (5),the resistor ratios determine β, and therefore the TC of the resistances has little influence on the voltage V_5 by using the same type of resistor.

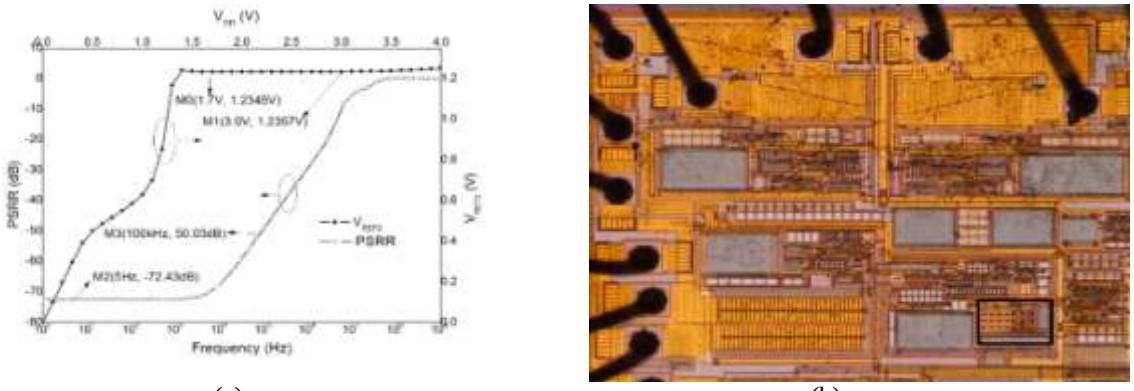
III. SIMULATION AND EXPERIMENTAL RESULTS

The proposed circuit is simulated by using Cadence Spectre based on SMIC 0.18μm CMOS process. The simulation results are presented in Fig. 3 and Fig. 4 (a).Fig. 3(a) shows the FCBGR voltage and SCC simulation wave forms at 2.0 V. We can see that they have opposite curvature characteristic. Therefore, the compensation voltage generated by SCC flows through the linear resistance can be effectively used to compensate FCBGR voltage. As shown in Fig. 3 (b), the TC of the reference voltage after compensation can reach 0.6 ppm/°C. In Fig. 4 (a), the presented BGR voltage deviation is about1.2 mV with the power supply ranging from 1.7 to 3.0 V. Moreover, the PSRR is about -72 dB at 10 Hz and -50dB at 100 kHz.



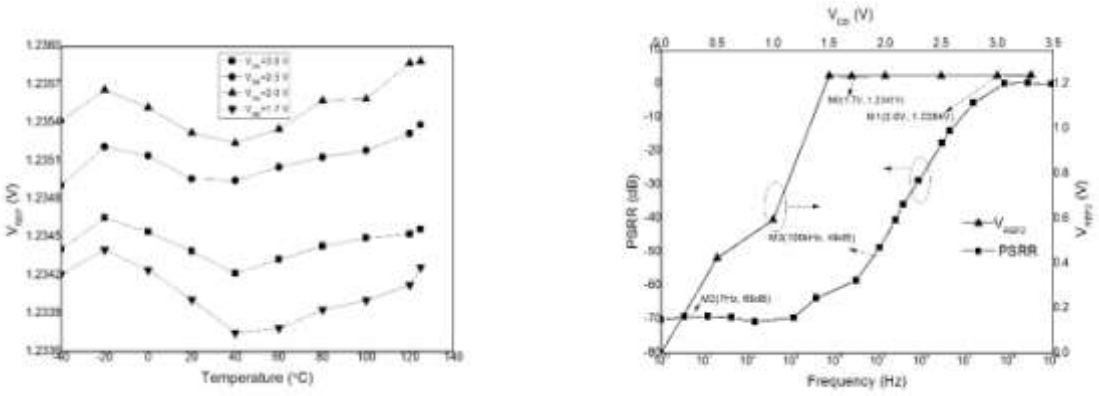
(a) (b)

Fig. 3. (a) VREF1 and SCC versus temperature; (b) VREF2 versus temperature.



(a) (b)

Fig. 4. (a) Simulated line sensitivity and PSRR results; (b) Chip micrograph of PMU (the BGR is in the rectangle).



(a) (b)

Fig. 5. (a) Measured temperature dependence of the BGR; (b)Measured line sensitivity and PSRR results.

The proposed BGR embedded intoPMU chip is implemented in SMIC 0.18μm CMOS process with effective chip area of 0.05 mm2 and providesa BGR voltagefor the entiresystem. The chip microphotograph of PMU is presented in Fig. 4 (b) and the BGR is in the rectangle. For the purpose of reducing the process mismatch effect, the common-centroid means is used for the layout of BJTs and MOS transistors, where 1BJT of Q1 is symmetrically surrounded by 8 BJT of Q2. In order to get accurate test results, each measurement is repeated ten times by alternating probes at a temperature point, then their average as the final result. The measured results are presented in Fig. 5.Fig. 5 (a) demonstrates the measured reference voltages at different supply voltages. In the temperature ranging from -40 to 125℃, the best TC is up to 2.2 ppm/℃ at the supply voltage of 2.0 V. The worst TC is 3.4 ppm/°C at the supply voltage of 1.7 V. InFig. 5 (b), while the supply voltage varies between 1.7and3.0V, the reference voltage deviation is 1.3mVand power regulation is about1mV / V.Thus, the proposed compensation principle is able to achieve the voltage reference which is almost independent of temperature and supply voltage. Furthermore, the PSRR is -69 dB at low frequency (less than 100 Hz) and -49dB at 100 kHz. The result reveals the designed BGR has a good PSRR.Thus, the BGR circuit can effectively suppress the output voltage changes caused by the supply variations.

Table 1. Performance comparison with the reported CMOS voltage reference circuits.

	This work	Ref.[6]	Ref.[5]	Ref.[10]
Technology	0.18μmCMOS	0.13μm CMOS	0.35μm CMOS	0.18μm CMOS
Supply voltage / V	2.0	1.2	1.85	0.7/1.2
Reference voltage / V	1.23	0.735	0.9055	0.548/1.09
Temperature coefficient/ ppm/℃	2.2	4.2	14.8	114/147
Temperature range/℃	-40~125	-40~120	0~100	-40~120
PSRR/dB	-69	-30	-61	-62/-56
Chip Area/mm^2	0.05	0.13	0.01	N.A.

Table I. summarizes the performances of the designed BGR and compares their characteristics with the previously proposed circuits. Compared with other CMOS voltage references circuits, the presented circuit shows better TC and PSRR. Temperature range of this circuit is wider than other three circuits. Therefore, the proposed circuit can be used in the systems mentioned in the introduction.

IV. CONCLUSION

This paper presents a high-precision BGR without using an op-amp, which can be implemented by the standard 0.18μm CMOS process. By using the Lambert W function, a theoretical analysis of the proposed curvature-compensated technique is performed. The presented circuit achieves an improved measured performance with comparisons to other previously proposed BGR's. It achieves2.2 ppm/°C in the range of -40°C to 125°C at 2.0 V power supply and its PSRR is -69 dB. In the range of 1.7 to 3.0 V, the maximum TC is 3.4 ppm/°C, the deviation of the presented BGR voltage is about 1.3 mV and the power regulation is about 1mV

/ V. This circuit can produce a stable 1.23 V output voltage. Therefore, the designed BGR can be used for systems neededhigh-precision reference.

V. Acknowledgement

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